arithmetic logic unit, and first and second clock generators. The multiplier includes an output port that operates under the control of the second clock and is coupled to provide data to a first input port of an adder. The adder includes both a first input port and second input port, both operating under the control of the second clock. A first and second input port of the multiplier and an output port of the adder operate under the control of the first clock. During a first clock cycle, a first operation is performed on a first operand and on a second operand in the multiplier of the first clock cycle. An adder is loaded with a result of the first operation and a fourth operand, and a second operation is performed in a second clock cycle by the adder by a second clock generated by the first clock. This is a distinctly different operation from Applicants' claimed invention.

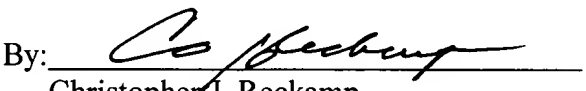
For example, the Office Action cites column 22, lines 25-30 as allegedly teaching, among other things, combining a second set of operands using the first operation unit during the second cycle to produce a second operation result. Claim 12 also requires, for example, combining a first set of operands using a first operation unit during the first clock cycle to produce the first operation result. Hence, the first operation unit is used to perform a combination of the first set of operands and a later combining of the second set of operands during the second cycle. However, the cited portion of the Ahsan reference indicates that two different operation units are being used, namely a multiplier and an adder. In contrast, Applicants respectfully note that the claim requires that the same operation unit perform the combining of the first set and second set of operands during a first and second clock cycle respectively. Accordingly, claims 12 and 13 are believed to be in condition for allowance.

Moreover, the Office Action admits that Ahsan does not disclose, among other things, selecting a first operand of a third set of operands from a set of potential operands that include the buffered first operation result, wherein selecting the first operand of the third set of operands occurs during a third cycle, wherein selecting the first operand of the third set of operands is based on the current op code and combining the second operation results and the buffered first operation result using a second operation unit during a third cycle to produce a third operation result. It appears that the Kanekura reference has been cited as teaching such an operation. However, Applicants respectfully note that the Kanekura is directed to a digital signal processing operation apparatus. The Office Action cites column 4, lines 65-66 and column 5, lines 19-21,

However, Applicants respectfully note that these cited portions merely indicate that a selector responsive to a selection signal can select input data from an adder-subtractor to provide the information to a shifter. There is no teaching or suggestion of combining or of selecting a first operand or a third set of operands from a set of potential operands that includes the buffered first operation result. It appears that Kanekura is silent as to any buffering. Moreover, Kanekura is silent as to combining the second operation result and the buffered first operation result using a second operation unit during the third cycle to produce a third operation result. Applicants are unable to find such a teaching in Kanekura and if the claim is not allowed, Applicants respectfully request a showing as to column and line number of such a teaching of the cited reference.

Accordingly, Applicants respectfully submit that the Claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: 
Christopher J. Reckamp
Registration No. 34,414

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Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
(312) 609-7599
FAX: (312) 609-5005